

# Proposal for MOSIS Educational Program funding (Research)

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## 1 Project description

High-speed digital design is becoming increasingly analog. In particular, interconnect response at high frequencies can be nonmonotonic, producing "porch steps" and ringing in signal lines. Crosstalk (both capacitive and inductive) can result in glitches on wires that can produce functional failures in receiving circuits. Most of these important effects are not addressed with traditional ATPG and BIST techniques, which are limited to the binary abstraction. In this chip, we explore the feasibility of integrating primitive sampling oscilloscopes on-chip to provide waveforms on selective critical nets for test and diagnosis. The oscilloscopes rely on subsampling techniques to achieve sub-10 psec timing accuracy. High speed samplers are combined with DLLs and a simple 8-bit ADC to convert the waveforms into digital data that can be incorporated as part of the chip scan chain. These samplers and measurement circuits are applied to a 4-mm 16-bit on-chip bus structure to consider crosstalk noise and inductive effects in the bus. The interconnect structure is also duplicated two additional times in configurations that will allow probing with Cascade probes for external S-parameter measurement with a vector network analyzer.

## 2 Project specs

The project size is approximately  $2.4 \text{ mm} \times 3.5 \text{ mm}$  in TSMC  $0.25 \mu\text{m}$  Mixed-Signal process. Of the 40 parts, 25 will be packaged in LCC84M and 15 will be unpackaged for Cascade probing on the probe station.

## 3 Simulation plans

The design has been extensively simulated in HSPICE and Powermill. The interconnect structures was been extracted in Ansoft's HFSS and Cadence's Assura RCX.

## 4 Test and characterization plans

The design will be clocked with an Agilent 81131A pulse-pattern generator. The DLL outputs will be measured with an Agilent 54750A sampling oscilloscope. The on-chip test circuits will be tested with the logic analyzer and digital pattern generator.

The separate interconnect structures will be probed with the Cascade probes and the vector network analyzer (to extract S parameters).