

Radio-Frequency Research and Education Programme: Design of Bluetooth Receivers

A Research/Educational Proposal

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Rationale and Goals

The RF (radio frequency) and the wireless market are growing at an unimaginable dimension. Products like pagers, cellular phones, GPS and satellite networks are rapidly penetrating all the aspects of the modern life making new advanced technological products indispensable tools. A new aspect that will enhance further the use of RF wireless devices is the use of the ISM band 2.4-2.5 GHz for very short distance communication. This opportunity is made possible by the advancement of the IC technology, namely the commercial availability of sub-micron CMOS. However, a potential risk to development exists: the shortage of designers and engineers with a proper background.

This proposal addresses the above problem and wants to achieve the following goals:

- To design all the key components required in typical Bluetooth architectures.
- To perform analysis and computer simulations of possible Bluetooth architectures.
- To assemble the basic components and integrate two specific architectures.
- To measure and assess the architectures for possible practical applications.

Therefore, more in general, the proposal wants to:

- To enhance the design capability of the AMSC in the RF area.
- To enhance the team-work capability of graduate students.
- To create the basis for a future research activity on Bluetooth applications for biomedical applications, wireless computer interconnections, wireless sensor networking.

Background of the Group

Twelve students currently form the RF and baseband group. The group has previous experience in the design and testing of LNAs, Mixers, VCOs, Power Amplifiers, Filters, AGCs and ADCs. The system and transistor level design of a subsampling receiver has been done.

Project Description

Bluetooth Technology

Bluetooth is a new technology for small-form factor, low-cost, short-range radio links between mobile PCs, mobile phones and other portable devices. It is believed to be the fastest growing industry standard ever. The objective of the project is to design, layout, and characterize the performance of a fully integrated Bluetooth receiver. Two different receiver architectures are being designed: direct conversion and low IF. Both architectures will be compared from the performance and cost point of view. Due to the high frequency utilized by Bluetooth technology, 2.4 GHz, large-scale process like 1.2 μm , 0.5 μm , will limit the receiver performance due to low f_T . Thus, the access to a small-scale process, 0.35 μm , would allow us to obtain a competitive performance of the receiver. Another goal of this project is to demonstrate that CMOS process can be used to design high performance RF circuits. The design of the receiver is the result of a team effort, thus the benefits of the experience obtained during the design and testing of the circuit will be shared among a large group of students. The group teaches a course on RF CMOS circuits and systems, this course requires a parallel laboratory. Currently, the lab involves the simulation of communication

systems building blocks as LNA's and Mixer. The availability of a receiver would enhance the laboratory level by allowing the students to perform several kind of tests such as noise figure, linearity, etc.

Simulation and Layout Plans

First, the system level design is carried out by using HPADS, Matlab and Simulink. The goal is to decide the best receiver architecture, and obtain the specifications of the different blocks in the receiver. Even in the system level simulation, we have tried to include the possible non-idealities caused by the process variation, like the mismatch etc.

Then, transistor level design will be simulated using SpectreRF (Cadence). This will be done using the SPICE model parameters provided by MOSIS for the 0.35 μ m technology. At this stage, the difference between required specifications and simulated results should be justified. Monte Carlo simulation is also required to ensure that the design is robust enough to meet the specifications under normal manufacturing process variations. This will provide us with an estimated distribution of the values of the most important specifications as a function of the statistically varying device model parameters. A buffer will be placed at the output of each block and any node which is wanted to be testable so that the performance of the whole receiver can be tested. Also each block can be tested independently, thus in case one block does not work due to any reason, we can still measure the other blocks. In addition, since the design is at very high frequency, the effect of bond wire, package and parasitic capacitance caused by the metal line need to be taken into account, this can be done by proper macromodeling.

Next, a layout of the final design will be created using Virtuoso Environment of Cadence. Good layout techniques such as common-centroid arrangements and dummy transistors should be used for better matching. The LVS (Layout vs. Schematic) checker tool of Cadence will be used to ensure that both the extracted layout and the schematic are matched. For our application, the parasitic become of extreme importance as they can affect the performance of the high frequency circuit seriously. So it becomes a must in this stage to perform postlayout simulation of the design using the extracted layout including the parasitic rather than the circuit schematic used in the first stage. This will give us a prediction of the effect of the parasitic on the performance of the design. It is also important to mention that we are also intending to include in our layout, beside the main design, a bank of single transistors of different sizes. This will allow us to extract the most important model parameters (such as the intrinsic transconductance and the threshold voltage) through testing measurements and compare them with the ones provided by MOSIS.

Test Plans

The final stage will be the characterization of the fabricated chip. A careful set up for measurements is needed. In high frequency circuits, the performance becomes sensitive to both the resistive and capacitive loading of the measuring equipment. A buffer has to be included instead of directly measuring the output. This will be included in the original layout. To fully characterize the transfer function of the buffer along with the connection pads, a separate buffer will be included to estimate its transfer function and then consider it while determining the performance of the original design for more accurate results.

In order to fully characterize the receiver, noise figure, gain, 1dB compression point and IP3 have to be measured in the RF section and gain, distortion and integrated noise in the IF/Baseband section. Phase noise measurements, settling time and spurs measurements are needed to characterize the frequency synthesizer. The input matching of the LNA will be verified with the Network Analyzer HP 8719ES, the frequency range of the analyzer goes from 50MHz to 13.5GHz. The measurements will be carried out using the Rohde & Schwarz Spectrum Analyzer FSEB that operates from 20Hz to 7GHz. Two signal generators are needed to generate the test signals, one to measure noise figure, 1 dB compression point and gain, and two to measure the IP3. The HP 8648C Signal Generator, which works from 9kHz to 3.2GHz, and the Rohde & Schwarz SMIQ Signal Generator, which works from 300kHz to 3.3GHz, will be used to generate the proper test signals.

The group has a probe station that will be used to test some unpackaged samples of the chip allowing us to obtain more accurate measurements of the circuit performance. The desired packaging is TQFP, with 144 pins, to minimize the effect of packaging and bond wire parasitics.

Project Schedule

The Project is divided in different phases. It is based on preliminary study and literature search performed by the team of graduate students involved in the project. The expected duration is 8 months. The following Table shows the Project schedule.

Task	Description	May	Jun	July	Aug	Sept	Oct	Nov	Dec
1	System design. Specification of blocks	X	X						
2	Basic blocks design		X	X					
3	Basic blocks validation			X	X				
4	Architecture analysis	X	X	X	X				
5	Layout of blocks				X	X			
6	Testing procedures						X	X	
7	Layout of architectures					X			
8	Fabrication						X	X	
9	Testing set-up						X	X	
10	Measurements								X

Milestones and Deliverables

Task	Description	May	Jun	July	Aug	Sept	Oct	Nov	Dec
1-3	Report on basic block design				X				
4	Report on Architectures				X				
6	Testing procedure						X		
9	PCB for testing							X	
10	Report on measurements								X
1-10	Final team report								X
1-10	Seminar on achieved results and progress report				X		X		X

Estimated Project Size

Since we are planning to integrate two different architectures on the same chip, the required silicon area is large. The LNA and VCO require the use of on-chip inductors, which occupy a large amount of area. The frequency synthesizer consumes a large area due to the large capacitors needed in the lowpass filter. Besides, we want to test some of the blocks independently, which doubles the area needed for them.

The estimated silicon area needed for this project is: 6mm × 6 mm

Students involved

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