A Proposal for a
MOSIS Research Account

Submitted by:
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**Design, Simulation, Layout, Fabrication, and Testing of a 2nd Order, Low-Pass, MOSFET-C Filter**

## Project Description

This project is to design, simulate, layout, and test a 2nd-order, low-pass, MOSFET-C, continuous time, analog filter using CMOS transistors. The filter is designed using the MOSIS 0.5? CMOS model parameters in anticipation of being fabricated by the MOSIS Research program.

The filter design utilizes the Tow-Thomas biquad circuit configuration with MOSFET transistors replacing the resistors used in the traditional version of the circuit. A four-transistor, differential arrangement of the MOSFETs is used to minimize nonlinearities[1]. A proven operational amplifier design is used for the three op-amps in the circuit. The op-amp design was part of a previous student MSEE project that was fabricated using the MOSIS 0.5? technology. The capacitors use an four-layer interleave configuration that utilizes the metal 1, metal 2, poly 1, and poly 2 layers.

The chip area and package pins will be fully utilized by including various sub-circuits of the full design to aid in the test and characterization. Critical internal nodes of the circuit will also be connected to the package pins for testing and characterization.

The project will form the major portion of an MSEE thesis for Mr. Voon-Kit Chea and will be supervised by Professor Jerry Yeargan.

Dr. Yeargan has taught graduate and undergraduate courses and conducted research in analog electronics since 1982. He conducts a graduate program in Mixed-Signal and Linear Microelectronics that typically graduates 4-6 students per year.

Mr. Chea has completed courses in

- ?? ELEG 4243- Analog Integrated Circuit Design (Text: Analog Integrated Circuit Design, by David A. Johns and Ken Martin),
- ?? ELEG 4883-Mixed-Signal IC Test and Measurement (Text: An Introduction to Mixed-Signal IC Test and Measurement, by Mark Burns and Gordon Roberts), (This course had a laboratory content
- ?? ELEG 4233-Introduction to Integrated Circuit Design, (Text: Principle of CMOS VLSI Design, by Neil Weste and Kamran Eshragian), and

[1] M. Banu and Y. Tsividis, "Fully-integrated active-RC Filters in MOS technology," IEEE Journal of Solid-State Circuits, SC-18, pp 644-651, Dec. 1983.

?? ELEG 5263L-Integrated Circuit Design Laboratory I (Text: Mentor Graphics Manuals) Mr. Chea designed a circuit in this class that was fabricated by MOSIS.

**Estimated Project Size**

The circuit will be designed to fit on a 1.5mm X 1.5mm chip.

**Simulation Plans**

Orcad Capture will be used for the circuit schematic layout and design and Orcad PSPICE version 9.2 (full version) will be used to verify that the design meets specifications and to simulate the circuit for bias conditions, frequency response and stability, and transient response and settling time. The BSIM (PSPICE Level 8) model with MOSIS supplied model parameters is used for the CMOS transistors. A major portion of the design simulation will be to investigate nonlinearities in the signal created by the use of the MOSFET's biased in the triode region. Mentor Graphics software is used for layout and to estimate parasitics and to verify chip layout.

**Test and Characterization Plans**

The fabricated chip will be tested and characterized using the following equipment
HP E3613A – triple output dc power supply,
Agilent 33120A – 15MHz function/arbitrary waveform generator,
Tektronix TDS 520C 500 MHz oscilloscope,
Hewlett Packard 54645D 100 MHz, mixed-signal oscilloscope,
Rucker and Kolls Model E683A probe station with GGB 200 MHz picoprobes,
Gateway E4200 and Professional models PC's equipped with National Instruments Labview version 6.0 and Orcad PSPICE version 9.2.
(Other equipment including high-frequency network analyzers and spectrum analyzers are available if needed.)

Tests on the fabricated chip will include

1. DC bias conditions
2. Input offset voltage
3. Frequency Response including bandwidth, rolloff, distortion, and unity gain frequency.
4. Input and output signal range
5. Transient Response and Settling Time

Major objectives of the tests are to determine and explain measured performance as compared to the design and simulated performances, and the effect of the nonlinearities created by the MOSFETs operating in the triode region.